REMARKS

Present Status of the Application

The Office Action rejected all pending claims 1-20. Specifically, the Office Action rejected claims 1-4 and 6-13 under 35 U.S.C. 102(e) as being anticipated by Sato (U. S. publication 2002/0140645). The Office Action also rejected claims 5 and 14-20 under 35 U.S.C. 103(a) as being unpatentable over Sato. Applicant has amended claims 1 and 12 to improve clarity. Applicant has also amended specification to correct typographic errors. After entry of amendments, claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejected claims 1-4 and 6-13 under 35 U.S.C. 102(e) as being anticipated by Sato. Applicant respectfully traverses the rejections for at least the reasons set forth below.

As shown in FIG. 6 of the present invention, the clock CLK1 is partitioned into the clocks CLK2A and CLK2B. For the clock, the clock is defined that several operation pulses are generated by a period. The period is larger than the pulse width of the clock. The clock in the present invention is not a conventional clock with half period at high state and half period at low state. For this clock, the first clock can be partitioned. In other words, there are two pulses in one period.

With respect to independent claim 1, based on the two clocks CLK2A and CLK2B, data

signals are input to the driver circuit at first clock, such as CLK2A, and the reset signals are input to the driver circuit at second clock. These features are clearly recited in independent claim 1 as follows:

> 1. A driving method for a light-emitting device, suitable for use in an active matrix light-emitting display, comprising:
> providing a driver circuit to control the light-emitting device, the driver circuit comprising a data input terminal for inputting a data signal, so as to control the light-emitting status of the light-emitting device;
> ***providing a clock and partitioning the clock into a first clock and a second clock, wherein the first and the second clocks have the same frequencies but are asynchronous to each other;***
> ***inputting the data signal to the data input terminal of the driver circuit at the first clock; and***
> ***inputting the reset signal to the data input terminal of the driver circuit at the second clock,***
> ***wherein each of the clocks is defined that operation pulses are sequentially issue by a period, wherein the period is larger than a pulse width of the operation pulses*** *(emphasis added).*

The features emphasized above are at least not disclosed by Sato.

In other words, the first clock is used to normally display the frame. The second clock is used to discharge the frames, so as to reset the driving TFT in threshold voltage (Vt). The phenomenon of Vt shift is reduced in the present invention.

In re Sato, the Vt shift of the driving TFT is not considered. The operation described in paragraphs [0095] and [0096] does not disclose the foregoing features of the present invention.

Moreover, in Fig. 3 and Fig. 4 of Sato (comparing with FIG. 3 of the present invention), the clocks CLK+ and CLK- are ***totally complementary to each other*** with half period at high state and half period at low state. The DATA signal (see Fig. 4) is not input based on one of the

clocks CLK+ and CLK-. The reset signal is not disclosed to input to the driver circuit based on another one of the clocks CLK+ and CLK-.

Clearly, the clocks CLK+ and CLK- of Sato failed to disclose the features recited in claim 1.

With respect to independent claim 12, in addition to at least the same foregoing reasons, independent claim 12 alternatively recites that ***the reset signal in a fixed frequency is applied to the display during each display frame.*** In other words, for each display frame, a reset signal with fixed frequency is applied to the pixel cells. The features are recited in independent claim 12 as follows:

> 12. A driving method for a light-emitting device, applicable to an active matrix light-emitting display system that includes a video control unit receiving a continuous video signal with a frame as the unit, the frame being input with an image display clock, wherein the image display clock outputs an image signal to an active matrix light-emitting display via a clock control unit after performing a decoding and signal process, the driving method comprising:
>
> *after the clock control unit outputs the image signal and before the frame is changed,* ***a reset signal, with a fixed clock frequency, corresponding to the frame is output to the active matrix light-emitting display to temporarily switch off a plurality of pixel units corresponding to the frame, wherein the pixel units use one frame as the unit to display an image of the frame*** (*Emphasis added*).

The reset signal can be the clock CLK2B in FIG. 3 of the present invention.

In re Sato [0088]-[0090], the signal ST is only disclosed as a start pulse ST. Sato never disclose that the start pulse ST is used to define the frame. Furthermore, the reset circuit RST is controlled by the signal R to reset the data signal, immediately in front of the each data line DL respectively provided [0089]. ***On contrary, the reset signal of the present invention is to***

temporarily switch off the pixel units corresponding to the frame. Clearly, with at least the foregoing reasons, independent claim 12 is distinguishable over Sato.

With at least the same foregoing reasons apples in claims 1 and 12, dependent claims 1-4, 6-11 and 13 are distinguish over Sato as well.

Discussion of Claim Rejections under 35 USC 103

The Office Action also rejected claims 5 and 14-20 under 35 U.S.C. 103(a) as being unpatentable over Sato. Applicant respectfully traverses the rejections for at least the reasons set forth below.

With at the same the foregoing reasons, Sato failed to disclose features of dependent claims 5 and 14-15.

With respect to independent claim 16, in addition to the same foregoing reasons applied to claims 1 and 12, the clock CLK+ and CLK- are not the first clock CLK2A and the second clock CLK2B. Also and, one of the clocks CLK2A and CLK2B is used as the rest clock to reset the pixel unit for each frame. In Fig. 4 of Sato, the reset signal R is not one of the clocks CLK+ or CLK-.

In conclusions, the present invention uses the reset signal to reset the pixel unit, particularly to switching off the driving transistor 102. As a result, the threshold of the transistor 102 is not raised, and lifetime or color displaying quality can be improved. The present invention also produces these unexpected result by arranging the claimed reset signal.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 12, and 16 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-11, 13-15, and 17-20 patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-20 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : July 21, 2004

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